Drawing Industry in through IEEE ROADMAPS

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If you work in the Industry....you might want to know

- The industry direction…
- What Technologies are coming in 3-5 years or longer
- What are the Roadblocks and possible Solutions

IEEE Roadmaps positioned to create this value

The IEEE Roadmaps committee coordinates…

- 4 published Roadmaps https://roadmaps.ieee.org
- Many more ‘on the horizon’

Each Roadmap brings together International experts…

- From the industry, academia, government, research entities
- Forms Working Groups
- Discusses Tech Trends
- Makes predictions for 5-10-15+ years
- Refreshed every 1-2 years

Identifies Technology Trends

- Serves as an **independent, unbiased REFERENCE resource**

Identify Gaps and "Brick Walls"

A Semiconductor & Devices Roadmap ["IRDS"]

- >1M views in 2022
- In the EU Chips Act
- In the Japan Chips Act
- Referenced in US Chips Act
- Many Presentations

https://irds.ieee.org

IEEE

IRDS example of Roadblocks

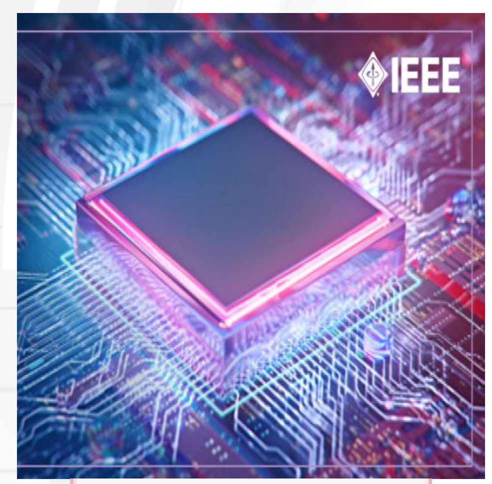
Table MM-7 Device Architecture and Ground Rules Roadmap for Logic Devices.

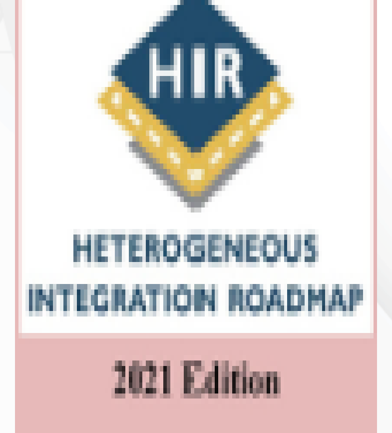
Note: GxxMxx/Tx notation refers to Gxx: contacted gate pitch, Mxx: tightest metal pitch in nm, Tx: number of tiers. This notation illustrates the technology pitch scaling capability. On top of pitch scaling there are other elements such as cell height, fin depopulation, DTCO constructs, 3D integration, etc. that define the target area scaling (gates/mm^2).

YEAR OF PRODUCTION	2021	2022	2025	2028	2031	2034
	G51M30	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Platform device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
	Drain Gate Source Oxide	Drain Gate Source Oxide	Drain Gate Source Oxide	Drain Gate Source Oxide	Drain Gate Source Oxide	Drain Gate Source Oxide
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	36	32	24	20	16	16
M1 pitch (nm)	34	32	23	21	20	19
M0 pitch (nm)	30	24	20	16	16	16
Gate pitch (nm)	51	48	45	42	40	38
Lg: Gate Length - HP (nm)	18	16	14	12	12	12
Lg: Gate Length - HD (nm)	20	18	14	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	7	6	5	4	4	4
Contact CD (nm) - finFET, LGAA	19	20	21	22	20	18
Contact CD (nm) - VGAA						
Device architecture key ground rules						
FinFET pitch (nm)	28.0	24.0				
FinFET Fin width (nm)	6.0	5.0				
FinFET Fin height (nm)	50	64				
Footprint drive efficiency - finFET	3.79	5.54				
Lateral GAA lateral pitch (nm)			22.0	20.0	20.0	20.0
Lateral GAA vertical pitch (nm)			18.0	16.0	14.0	14.0
Lateral GAA (nanosheet) thickness (nm)			7.0	6.0	5.0	5.0
Number of vertically stacked nanosheets			3	3	4	4
LGAA width (nm) - HP			30	25	20	15
LGAA width (nm) - HD			15	11	6	6
LGAA width (nm) - SRAM			7	6	6	6
LGAA total height (nm)			53	48	57	57
Footprint drive efficiency - lateral GAA - HP			4.93	4.77	5.88	5.52
Device effective width (nm) - HP	106.0	133.0	222.0	186.0	200.0	160.0
Device effective width (nm) - HD	106.0	133.0	132.0	102.0	88.0	88.0
Device lateral pitch (nm)	28	24	22	20	20	20
Device height (nm)	50.0	64.0	53.0	48.0	57.0	57.0
Device width (nm) - HP	6	5	30	25	20	15
Device width (nm) - HD	6	5	15	11	6	6
Device width (nm) - SRAM	6	5	7	6	6	6

Screenshot

A Heterogeneous Integration Roadmap ["HIR"]

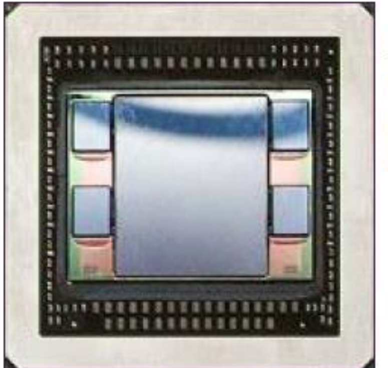




- Referenced in US Chips Act
- Many Presentations

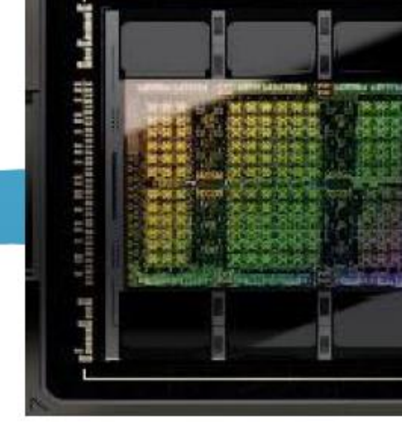
https://eps.ieee.org/technology/heterogeneous-integration-roadmap.htm

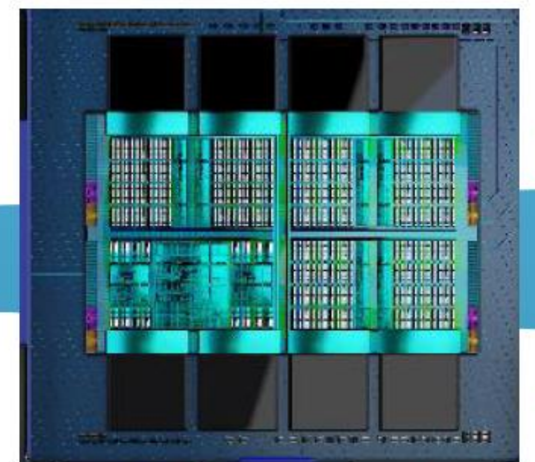
Examples of Multi-die Hi-performance Compute Servers



AMD:
Radeon R9
FURY X
(2015)

NVIDIA:
Tesla P100
(2016)





2023: AMD MI300
3GPU+1 CPU
8 HBM3

A “Chiplets” example…

Monolithic SoC

Modularized SoC (Chiplets)

AI/ML

NW Switch

Server

PC

Large FCBGA /MCM

2.5D Si TSV

HD FO RDL /Bridge

3D ubump/ Hybrid bond

Advanced packaging Heterogeneous Integration

Reference: "The March Towards Chiplets" Ed Sperling & Karen Heyman, December 15, 2022. Semiconductor Engineering

A Wide Bandgap Semiconductor Roadmap [“ITRW”]

https://resourcecenter.ieee-pels.org/roadmap/PELSPRO0020.html

A Network Generations Roadmap [“INGR”]

Applications and Services	Millimeter Wave and Signal Processing
Artificial Intelligence / Machine Learning	Optics
Connecting the Unconnected	Satellite
Deployment	Security and Privacy
Edge Services and Automation	Standardization Building Blocks
Energy Efficiency	Systems Optimization
Massive MIMO	Testbed

- >1.5k Views per month
- Many Presentations
  - >6 Conferences
  - 7 Webinars
  - 2 Technical Workshops
  - Podcast series
  - >2k registrants

https://futurenetworks.ieee.org/roadmap/

Present 5G has Many Limitations

- Limited range due to Spectrum mid- and high-band
- Limited mmWave integration
- Security and Privacy issues
- Limited deployment of Standalone mode
  - Limited thruput, latency etc.

Operators need a Testbed to evaluate 5G enhancements

A 5G/6G Innovation Testbed

...launched by IEEE Future Networks to enable the Industry

- **Test**
  - Efficient, economic 5G conformity testing within the 3GPP standards ecosystem
- **Experiment**
  - Flexible, scalable, and “always on” for proof-of-concept development within a wide range of 5G use cases and scenarios
- **Collaborate**
  - Partner with other companies to test compatibility or enhance quality of service in secure, private environments
- **Innovate**
  - Adjust, transform, and integrate new network functions or features

testbed.ieee.org

“On the horizon” Roadmaps

Int’l Tech Roadmap of Power Electronics for Distributed Energy Systems

Sustainable Energy

Other Roadmaps under way

Instrumentation & Measurements for Brain [or Healthcare Systems]

Smart Lighting

Telepresence

LEOS *(Lo Earth Orbit Satellites)*

Public Safety

Reliability

What can YOU do?

- **Participate** in the Development
- **Use** the Roadmaps
- Help industry participants **Develop** a Roadmap at their company using our methodology
  - ***Especially Young Professionals!!***

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